

What Is Claimed Is:

1 1. A method for using electrostatic forces to align semiconductor
2 chips relative to each other, comprising:
3 electrically charging a first set of conductors on a first chip;
4 electrically charging a second set of conductors on a second chip;
5 placing the first chip face-to-face with the second chip, so that the first set
6 of conductors is in close proximity to the second set of conductors; and
7 allowing electrostatic forces between the first set of conductors and the
8 second set of conductors to bring the first chip into alignment with the second
9 chip.

1 2. The method of claim 1, wherein the process of electrically charging
2 the first set of conductors and the second set of conductors takes place after the
3 first chip is placed face-to-face with the second chip.

1 3. The method of claim 1, wherein the process of electrically charging
2 the first set of conductors and the second set of conductors involves applying a
3 changing pattern of voltages to the first set of conductors and the second set of
4 conductors.

1 4. The method of claim 1, further comprising vibrating the first chip
2 and/or the second chip to facilitate aligning the first chip and the second chip.

1 5. The method of claim 1, further comprising applying a lubricant
2 between the first chip and the second chip to reduce frictional forces between the
3 first chip and the second chip during the alignment process.

- 1 6. The method of claim 1, wherein placing the first chip face-to-face
2 with the second chip involves using a mold as a guide to facilitate bringing the
3 first set of conductors in close proximity to the second set of conductors.
- 1 7. The method of claim 1, wherein a pattern formed by the first set of
2 conductors matches a pattern formed by the second set of conductors.
- 1 8. The method of claim 1, wherein the first set of conductors and the
2 second set of conductors are arranged in a checkerboard pattern.
- 1 9. The method of claim 1, wherein the first set of conductors and the
2 second set of conductors are arranged in a pattern of concentric circles.
- 1 10. The method of claim 1, wherein the first set of conductors and the
2 second set of conductors are arranged in a pattern with an autocorrelation
3 approaching an impulse.
- 1 11. The method of claim 1, wherein the electrostatic forces between
2 the first set of conductors and the second set of conductors include attractive
3 forces and/or repulsive forces.
- 1 12. The method of claim 11, wherein the electrostatic forces between
2 the first set of conductors and the second set of conductors generate a net
3 repulsive force that levitates the first chip over the second chip, thereby reducing
4 frictional forces between the first chip and the second chip.

1 13. The method of claim 1, wherein the first set of conductors
2 comprises part of a power network and/or a ground network of the first chip.

1 14. The method of claim 1, wherein electrically charging the first set of
2 conductors on the first chip involves charging different conductors to different
3 voltage levels.

1 15. The method of claim 1, wherein electrically charging the first set of
2 conductors involves using electron-implanted charges.

1 16. The method of claim 1, further comprising bonding the first chip
2 with the second chip after the first chip is brought into alignment with the second
3 chip.

1 17. An apparatus that facilitates using electrostatic forces to align
2 semiconductor chips relative to each other, comprising:
3 a charging mechanism configured to electrically charge a first set of
4 conductors on a first chip and a second set of conductors on a second chip; and
5 an initial placement mechanism configured to place the first chip face-to-
6 face with the second chip, so that the first set of conductors is in close proximity
7 to the second set of conductors;
8 whereby electrostatic forces between the first set of conductors and the
9 second set of conductors bring the first chip into alignment with the second chip.

1 18. The apparatus of claim 17, wherein the charging mechanism
2 operates after the first chip is placed face-to-face with the second chip.

1 19. The apparatus of claim 17, wherein the charging mechanism
2 applies a changing pattern of voltages to the first set of conductors and the second
3 set of conductors.

1 20. The apparatus of claim 17, further comprising a vibrating
2 mechanism configured to vibrate the first chip and/or the second chip to facilitate
3 aligning the first chip and the second chip.

1 21. The apparatus of claim 17, further comprising a lubricating
2 mechanism configured to apply a lubricant between the first chip and the second
3 chip to reduce frictional forces between the first chip and the second chip during
4 the alignment process.

1 22. The apparatus of claim 17, wherein the initial placement
2 mechanism is configured to use a mold as a guide to facilitate bringing the first set
3 of conductors in close proximity to the second set of conductors.

1 23. The apparatus of claim 17, wherein a pattern formed by the first set
2 of conductors matches a pattern formed by the second set of conductors.

1 24. The apparatus of claim 17, wherein the first set of conductors and
2 the second set of conductors are arranged in a checkerboard pattern.

1 25. The apparatus of claim 17, wherein the first set of conductors and
2 the second set of conductors are arranged in a pattern of concentric circles.

1 26. The apparatus of claim 17, wherein the first set of conductors and
2 the second set of conductors are arranged in a pattern with an autocorrelation
3 approaching an impulse.

1 27. The apparatus of claim 17, wherein the electrostatic forces between
2 the first set of conductors and the second set of conductors include attractive
3 forces and/or repulsive forces.

1 28. The apparatus of claim 27, wherein the electrostatic forces between
2 the first set of conductors and the second set of conductors generate a net
3 repulsive force that levitates the first chip over the second chip, thereby reducing
4 frictional forces between the first chip and the second chip.

1 29. The apparatus of claim 17, wherein the first set of conductors
2 comprises part of a power network and/or a ground network of the first chip.

1 30. The apparatus of claim 17, wherein the charging mechanism is
2 configured to charge different conductors to different voltage levels.

1 31. The apparatus of claim 17, wherein the charging mechanism is
2 configured to use electron-implanted charges.

1 32. The apparatus of claim 17, further comprising a bonding
2 mechanism that is configured to bond the first chip with the second chip after the
3 first chip is brought into alignment with the second chip.

1 33. A means for using electrostatic forces to align semiconductor chips
2 relative to each other, comprising:
3 a charging means for electrically charging a first set of conductors on a
4 first chip and a second set of conductors on a second chip; and
5 an initial placement means for placing the first chip face-to-face with the
6 second chip, so that the first set of conductors is in close proximity to the second
7 set of conductors;
8 whereby electrostatic forces between the first set of conductors and the
9 second set of conductors bring the first chip into alignment with the second chip.